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PATENT APPLICATION

ATTORNEY DOCKET NO. 200310842-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Peter J. Fricke et al.

Application No.: 10/772,945

Filing Date: February 4, 2004

Confirmation No.: 5316

Examiner: NADAV, Ori

Group Art Unit: 2811

Title: Memory Array with Two-Terminal Crosspoints Using Silicon-Rich Insulator

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on June 3, 2008.

☒ The fee for filing this Appeal Brief is $510.00 (37 CFR 41.20).

☐ No Additional Fee Required.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120	☐ 2nd Month $460	☐ 3rd Month $1050	☐ 4th Month $1640

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 510 . At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees.

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Signature:

Respectfully submitted,
Peter J. Fricke et al.
By

Steven L. Nichols
Attorney/Agent for Applicant(s)
Reg No. : 40,326
Date : July 30, 2008
Telephone : 801-572-8066

Rev 10/07(ApiBrief)

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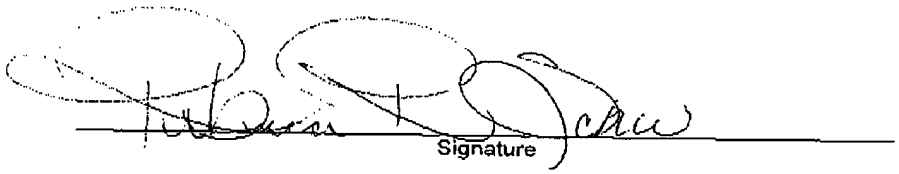

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Transmitted, herewith, are the following documents:

1. Transmittal of Appeal Brief with Duplicate Copy (2 pages)
2. Certificate of Transmission (1 page)
3. Appeal Brief (47 pages)

200310842-1

10/772,945

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Patent Application of

Peter J. Fricke et al.

Application No. 10/772,945

Filed: February 4, 2004

For: Memory Array with Two-Terminal Crosspoints Using Silicon-Rich Insulator (as amended)

Group Art Unit: 2811

Examiner: NADAV, Ori

Confirmation No.: 5316

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an Appeal Brief under Rule 41.37 appealing the decision of the Primary Examiner dated April 10, 2008 (the "final Office Action" or "Action"). Each of the topics required by Rule 41.37 is presented herewith and is labeled appropriately.

I. Real Party in Interest

The real party in interest is Hewlett-Packard Development Company, LP, a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

II. Related Appeals and Interferences

There are no appeals or interferences related to the present application of which the Appellant is aware.

III. Status of Claims

Claims 7, 34 and 35 have been previously cancelled without prejudice or disclaimer.

Claims 2, 12-15, 17-25, 36, 37, 42-46 and 50-54 have been withdrawn from consideration but remain at issue because they are subject to rejoinder upon the allowance of a pending independent claim.

Claims 1, 3-6, 8-11, 16, 26-33, 38-41, 47-49 and 55-59 are pending in the application and stand finally rejected.

Accordingly, Appellant appeals from the final rejection of claims 1, 3-6, 8-11, 16, 26-33, 38-41, 47-49 and 55-59, which claims are presented in the Appendix.

IV. Status of Amendments

No amendments have been filed subsequent to the final Office Action of April 10, 2008, from which Appellant takes this appeal.

V. Summary of Claimed Subject Matter

The present application discloses a memory array comprising a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points. (*Appellants' specification, Abstract*). A memory cell is disposed at each cross-point, each memory cell having a storage element and a control element coupled in series between a row conductor and a column conductor, and each control element including a silicon-rich insulator. (*Appellants' specification, Abstract*).

The layer (60) of silicon-rich insulator, for example a silicon-rich oxide (SRO), of the control element (45) provides for enhanced current injection into the dielectric of a tunnel junction layer (70). (*Appellants' specification, paragraph 0034*). Other advantages include improved isolation of each memory cell within the memory array thus resulting in significant reduction of cumulative sneak-path currents. (*Appellants' specification, paragraph 0035*). Still other advantages may include increased size of sub-arrays, lower manufacturing costs, ease of manufacturing without incurring destruction to other elements, increased compatibility with other devices, ability to produce devices having dimensions below 0.5 micrometers, and the silicon-rich insulator's ability to act like a control element due to its asymmetric rectification characteristics. (*Appellants' specification, paragraphs 0034-0036*).

Turning to Appellant's specific claims,

Claim 1 recites:

A memory array (10) comprising:

a) a multiplicity of row conductors (30) and a multiplicity of column conductors (40), the row conductors (30) and column conductors (40) being arranged to cross at cross-points, (*Appellants' specification, paragraphs 0028, 0033 and, 0062*) and

b) a memory cell (20) disposed at each cross-point, each memory cell (20) having exactly two terminals (*Appellants' specification, paragraphs 0039, 0051, and 0052, and Figs. 3, 14, and 15*) and having a storage element (50) and a control element (45) coupled in series between a row conductor (30) and a column conductor (40), each control element (45) including a tunnel junction (70) and a silicon-rich insulator (60) (*Appellants' specification, paragraphs 0031 and 0033*), wherein the silicon-rich insulator (60) injects current into the tunnel junction (70) when the memory cell (20) is selected (*Appellants' specification, paragraph 0034*).

Claim 16 recites:

A memory array (10) comprising:

a) a multiplicity of row conductors (30) and a multiplicity of column conductors (40), the row conductors (30) and column conductors (40) being arranged to cross at cross-points (*Appellants' specification, paragraphs 0028, 0033 and, 0062*), and

b) a memory cell (20) disposed at each cross-point, each memory cell (20) having exactly two terminals (*Appellants' specification, paragraphs 0039, 0051, and 0052, and Figs. 3, 14, and 15*), each memory cell (20) comprising means for storing data (50) and means for controlling (45) the means for storing data, the means for storing data (50) and means for controlling (45) being coupled in series between a row conductor (30) and a column conductor (40), each means for controlling (45) including a tunnel junction (70) and a silicon-rich insulator (60) (*Appellants' specification, paragraphs 0031 and 0033*), wherein the silicon-rich insulator (60) injects current into the tunnel junction (70) when the memory cell (20) is selected (*Appellants' specification, paragraph 0034*).

Claim 26 recites:

A memory cell (20) made by a method comprising:

a) providing a substrate (300) (Step 10) (*Appellants' specification, paragraph 0055, and Fig. 16*),

b) depositing and patterning a first conductive layer (30 or 40) over the substrate (300) (Steps 20 and 30) (*Appellants' specification, paragraph 0056, and Fig. 16*),

c) forming a storage layer (50) over the patterned first conductive layer (30 or 40) (Step 40) (*Appellants' specification, paragraph 0056, and Fig. 16*),

d) forming a layer of silicon-rich insulator (60) over the storage layer (50) (Step 50) (*Appellants' specification, paragraph 0056, and Fig. 16*),

e) forming a tunnel-junction layer (70) over the layer of silicon-rich insulator (60) (Step 60) (*Appellants' specification, paragraph 0056, and Fig. 16*), and

f) forming and patterning a second conductive layer (40 or 30) over the tunnel-junction layer (70) (Steps 70 and 80) (*Appellants' specification, paragraph 0056, and Fig. 16*), whereby a memory-cell stack is formed, the stack having a storage layer (50), a silicon-rich insulator (60), and a tunnel-junction layer (70) in series relationship between the first and second conductive layers (30 and 40) (*Appellants' specification, paragraphs 0055 and 0056*), whereby the first and second conductive layers (30 and 40) are adapted to provide exactly two terminals for control of the memory cell (20) (*Appellants' specification, paragraphs 0039, 0051, and 0052, and Figs. 3, 14, and 15*), wherein the silicon-rich insulator (60) injects current into the tunnel-junction layer (70) when the memory cell (20) is selected (*Appellants' specification, paragraph 0034*).

Claim 38 recites:

A memory cell (20) made by a method comprising:

a) providing a substrate (300) (Step 10) (*Appellants' specification, paragraph 0055, and Fig. 16*),

b) depositing and patterning a first conductive layer (30 or 40) over the substrate (300) (Steps 20 and 30) (*Appellants' specification, paragraph 0056, and Fig. 16*),

c) forming a storage layer (50) over the patterned first conductive layer (30 or 40) (Step 40) (*Appellants' specification, paragraph 0056, and Fig. 16*),

d) forming a layer of silicon-rich insulator (60) over the storage layer (50) (Step 50) (*Appellants' specification, paragraph 0056, and Fig. 16*),

e) forming a tunnel-junction layer (70) over the layer of silicon-rich insulator (60) (Step 60) (*Appellants' specification, paragraph 0056, and Fig. 16*),

f) forming and patterning a second conductive layer (40 or 30) over the tunnel-junction layer (70) (Steps 70 and 80) (*Appellants' specification, paragraph 0056, and Fig. 16*),

g) forming and patterning an interlayer dielectric (120, 340) over the storage layer (50) (Step 90) (*Appellants' specification, paragraphs 0058 and 0062, and Fig. 16, and Fig. 16*),

h) forming an opening through the interlayer dielectric (120, 340) and extending to the storage layer (50) (Step 100) (*Appellants' specification, paragraphs 0059, 0062, and 0063, and Fig. 16*), and

i) filling the opening through the interlayer dielectric (120, 340) with conductive material to form a middle electrode (130) contiguous with the storage layer (50) (Step 100) (*Appellants' specification, paragraphs 0059, 0062, and 0063, and Fig. 16*), wherein the first and second conductive layers (30 or 40) are adapted to provide exactly two terminals for control of the memory cell (20) (*Appellants' specification, paragraphs 0039, 0051, and 0052, and Figs. 3, 14, and 15*), and wherein the silicon-rich insulator (60) injects current into the tunnel-junction layer (70) when the memory cell (20) is selected (*Appellants' specification, paragraph 0034*).

Claim 47 recites:

A multilayer memory (10) made by a method comprising:

a) providing a substrate (300) (Step 10) (*Appellants' specification, paragraph 0055, and Fig. 16*),

b) depositing and patterning a first conductive layer (30 or 40) over the substrate (300) (Steps 20 and 30) (*Appellants' specification, paragraph 0056*),

c) forming a storage layer (50) over the patterned first conductive layer (30 or 40) (Step 40) (*Appellants' specification, paragraph 0056, and Fig. 16*),

d) forming and patterning a first interlayer dielectric (120, 340) over the storage layer (50) (Step 90) (*Appellants' specification, paragraphs 0058 and 0062, and Fig. 16*),

e) forming an opening through the first interlayer dielectric (120, 340) and extending to the storage layer (50) (Step 100) (*Appellants' specification, paragraphs 0059, 0062, and 0063, and Fig. 16*),

f) filling the opening through the first interlayer dielectric (120, 340) with conductive material to form a middle electrode (130) (Step 100) (*Appellants' specification, paragraphs 0059, 0062, and 0063, and Fig. 16*),

g) forming a layer of silicon-rich insulator (60) over at least the first interlayer dielectric (120, 340), at least a portion of the silicon-rich insulator (60) being disposed contiguous with the middle electrode (130) (Step 100) (*Appellants' specification, paragraphs 0059, 0062, and 0063, and Fig. 16*),

h) forming a tunnel-junction layer (70) over the layer of silicon-rich insulator (60) (Step 60) (*Appellants' specification, paragraphs 0056, and Fig. 16*),

i) forming and patterning a second conductive layer (40 or 30) over the tunnel-junction layer (70) and disposed to overlay vertically at least a portion of the middle electrode (130) (*Appellants' specification, paragraphs 0056 and 0062*), whereby a portion of the

second conductive layer (40 or 30) is aligned with some portion of the middle electrode (130) (*Appellants' specification, paragraphs 0056, 0062 and 0065*), and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell (20) (*Appellants' specification, paragraphs 0039, 0051, and 0052, and Figs. 3, 14, and 15*), and wherein the silicon-rich insulator (60) injects current into the tunnel-junction layer (70) when the memory cell (20) is selected (*Appellants' specification, paragraph 0034*),

j) forming and patterning a second interlayer dielectric (120, 340) over the patterned second conductive layer (40 or 30), whereby a substrate (300) is formed for subsequent layers (Step 90) (*Appellants' specification, paragraphs 0058, 0062, and 0064*),

k) forming vias (350) as required through the second interlayer dielectric (120, 340) (*Appellants' specification, paragraphs 0048, 0064, and 0065*), and

l) repeating steps b) through k) until a desired number of memory array layers have been formed (*Appellants' specification, paragraph 0064*).

Claim 55 recites:

A multilayer memory (10) made by a method comprising:

a) providing a substrate (300) (Step 10) (*Appellants' specification, paragraph 0055, and Fig. 16*),

b) depositing and patterning a first conductive layer (30 or 40) over the substrate (300) (Steps 20 and 30) (*Appellants' specification, paragraph 0056, and Fig. 16*),

c) forming a tunnel-junction layer (70) over the first conductive layer (30 or 40) (Step 60) (*Appellants' specification, paragraphs 0041, 0056, and Figs. 5-8*),

d) forming a layer of silicon-rich insulator (60) over the tunnel-junction layer (70) (Step 50) (*Appellants' specification, paragraphs 0041 and 0056, and Figs. 5-8*),

e) forming and patterning a first interlayer dielectric (120, 340) over the layer of silicon-rich insulator (60) (Step 90) (*Appellants' specification, paragraphs 0041, 0058 and 0062, and Figs. 5-8*),

f) forming an opening through the first interlayer dielectric (120, 340) and extending to the layer of silicon-rich insulator (60) (Step 100) (*Appellants' specification, paragraphs 0059, 0062, and 0063, and Fig. 16*),

g) filling the opening through the first interlayer dielectric (120, 340) with conductive material to form a middle electrode (130), at least a portion of the middle electrode (130) being disposed contiguous with the silicon-rich insulator (60) (Step 100) (*Appellants' specification, paragraphs 0059, 0062, and 0063, and Fig. 16*),

h) forming a storage-element layer over the patterned first interlayer dielectric (120, 340) (Step 40) (*Appellants' specification, paragraph 0056, and Fig. 16*),

i) forming and patterning a second conductive layer (40 or 30) over the storage-element layer (Steps 70 and 80) (*Appellants' specification, paragraph 0056, and Fig. 16*), the patterned second conductive layer (40 or 30) being disposed to overlay vertically at least a portion of the middle electrode (130) (*Appellants' specification, paragraphs 0056, 0062, and 0065*), whereby a portion of the second conductive layer (40 or 30) is aligned with some portion of the middle electrode (130) (*Appellants' specification, paragraphs 0056, 0062, and 0065*), and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell (20) (*Appellants' specification, paragraphs 0039, 0051, and 0052, and Figs. 3, 14, and 15*), and wherein the silicon-rich

insulator (60) injects current into the tunnel-junction layer (70) when the memory cell (20) is selected (*Appellants' specification, paragraph 0034*),

j) forming and patterning a second interlayer dielectric (120, 340) over the patterned second conductive layer (40 or 30), whereby a substrate (300) is formed for subsequent layers (Step 90) (*Appellants' specification, paragraphs 0058, 0062, and 0064*),

k) forming vias (350) as required through the second interlayer dielectric (120, 340) (*Appellants' specification, paragraphs 0048, 0064, and 0065*), and

l) repeating steps b) through k) until a desired number of memory array layers have been formed (*Appellants' specification, paragraph 0064*).

VI. Grounds of Rejection to be Reviewed on Appeal

The final Office Action raised the following grounds of rejection.

(1) Claim 5 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

(2) Claims 1, 3-6, 8-11, 16, 26-33, 38-41, 47-49 and 55-59 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 4,476,547 to Miyasaka ("Mikyasaka") in view of U.S. Patent Application Publication No. 2005/0012126 to Udayakumar et al. ("Udayakumar").

According, Appellant hereby requests review of each of these grounds of rejection in the present appeal.

VII. Argument

(1) Claim 5 complies with 35 U.S.C. § 112, second paragraph:

The final Office Action rejects claim 5 as being indefinite under 35 U.S.C. § 112, second paragraph. Appellant respectfully disagrees. Claim 5 recites:

> The memory array of claim 1, wherein the control element of each memory cell further comprises a tunnel junction layer thickness of about 3 – 5 nanometers.

Specifically, the Action argues that the claimed "tunnel junction layer" is unclear "as to the structural relationship between the tunnel junction layer and the memory array." (Action, p. 2).

Claim 5 depends from claim 1. Claim 1 expressly recites a memory cell disposed at each cross-point between column and row conductors. According to claim 1, each memory cell comprises a storage element and a control element, "each control element including a tunnel junction." Claim 5 then recites that the layer of the tunnel junction has a thickness of about 3-5 nanometers. Consequently, the relationship between the tunnel junction and the memory array appears to be perfectly clear.

Therefore, the final Office Action has failed to indicate any indefiniteness in claim 5 under § 112, second paragraph. For at least these reasons, the rejection of claim 5 should not be sustained.

(2) Claims 1, 3-6, 8-11, 16, 26-33, 38-41, 47-49 and 55-59 are patentable over Miyasaka and Udayakumar:

Claim 1:

Claim 1 recites:

> A memory array comprising:
>
> a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and
>
> b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals and having a storage element and a control element coupled in series between a row conductor and a column conductor, each control element including a tunnel junction and *a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.*

(Emphasis added).

In contrast, Miyasaka and Udayakumar utterly fail to teach or suggest this subject matter. The final Office Action concedes the shortcomings of Miyasaka. Specifically, the final Office Action states that "Miyasaka does not teach that each control element including (sic) a tunnel junction and a silicon-rich oxide insulator." (final Office Action, p. 3).

Consequently, the Action cites Udayakumar. According to the final Office Action, Ukdaykumar teaches "a memory cell Cfe having exactly two terminals and having a storage element and a control element wherein the control element including (sic) a tunnel junction and a silicon-rich oxide insulator SILOX2." (final Office Action, p. 3)

However, Udayakumar does not teach or suggest a memory cell having a control element, wherein the control element includes a silicon-rich oxide layer, "*wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected*" as recited in claim 1. Neither of the cited references teach or suggest this subject matter.

Udayakumar generally teaches that "SILOX . . . situated above or directly over the ferroelectric capacitor structures operates as an effective barrier to the diffusion of hydrogen." (*See Udayakumar, paragraph 0007*). Udayakumar further states that SILOX is used to

"reduc[e] or mitigat[e] hydrogen-related ferroelectric degradation in stand-alone memory products or devices having embedded ferroelectric memory." (*See* Udayakumar, paragraph 0021. *See also* Udayakumar, paragraph 0023).

In other words, in each embodiment of the Udayakumar structure, the SILOX layer is simply employed as an overlying passivation layer. Udayakumar fails to disclose that this SILOX layer has any relationship or proximity with a tunnel junction. Udayakumar further fails to teach or suggest that the SILOX layer functions to inject current into a tunnel junction.

The only application of a silicon-rich insulator in the Udayakumar reference is in connection with another hydrogen barrier, aluminum oxide (AlOx), of which the "silicon rich silicon oxide (SILOX)" is applied. (*See* Udayakumar, paragraph 0036, and Figs. 4D and 4E). Udayakumar further discloses that this multilayer hydrogen barrier, comprising a first AlOx layer and second SILOX layer, is applied to the top of a ferroelectric capacitor as a passivation layer. (*Id.*). When located at that position within the Udayakumar device, the indicated passivation layer is incapable of injecting current into a tunnel junction.

Under the analysis required by *Graham v. John Deere*, 383 U.S. 1 (1966) to support a rejection under § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. In the present case, the scope and content of the prior art, as evidenced by Miyasaka and Udayakumar, did not include the claimed subject matter, particularly the claimed memory cell comprising a control element with a tunnel junction and a silicon-rich insulator that injects current into the tunnel junction when the memory cell is selected. This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because, the claimed subject matter provides features and advantages not known or available in 1 and its dependent claims under 35 U.S.C. § 103 and *Graham*.

Claim 4:

Claim 4 recites:

> The memory array of claim 1, wherein the silicon-rich insulator of each memory cell is *electrically isolated from the silicon-rich insulators of all other memory cells*.

(Emphasis added).

With regard to claim 4, the final Acton argues that the prior art device isolates one silicon-rich insulator from the silicon rich insulators of all other memory cells. However, the Action failed to cite to any support for this position in either of the prior art references, Miyasaka or Udayakumar.

To the contrary, when properly understood, Udayakumar discloses a continuous SILOX layer that is interrupted only by the connection of conductive via structures to an upper capacitor plate in order to provide for electrical contact between the via structures and an upper capacitor plate. (*See* Udayakumar, paragraph 0037, and Fig. 4G). Thus, the cited prior art clearly teaches away from the claimed silicon-rich insulators electrically isolated from a similar layer in all other memory cells as recited in claim 4. For at least this additional reason, the rejection of claim 4 should not be sustained.

Claim 6:

Claim 6 recites "wherein the storage element of each memory cell comprises an anti-fuse." The final Office Action fails to specifically address claim 6 and does not indicate how

or where this subject matter is taught or suggested by the prior art of record. Consequently, no *prima facie* case of obviousness has been made against claim 6, and the rejection of claim 6 should not be sustained.

Claims 9 and 10:

Claims 9 and 10 recite, respectively, that "the storage element of each memory cell comprises a state-change layer" and "wherein the state-change layer of the storage element comprises a chalcogenide." The final Office Action fails to specifically address claims 9 and 10 and does not indicate how or where this subject matter is taught or suggested by the prior art of record. Consequently, no *prima facie* case of obviousness has been made against claims 9 and 10, and the rejection of claims 9 and 10 should not be sustained.

Claim16:

Claim 16 recites:

> A memory array comprising:
>
> a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and
>
> b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals, each memory cell comprising means for storing data and means for controlling the means for storing data, the means for storing data and means for controlling being coupled in series between a row conductor and a column conductor, each means for controlling including a tunnel junction and *a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.*

(Emphasis added).

As demonstrated above in connection with claim 1, Miyasaka and Udayakumar utterly fail to teach or suggest this subject matter of a "silicon-rich insulator [that] injects current into the tunnel junction when the memory cell is selected."

Under the analysis required by *Graham v. John Deere*, 383 U.S. 1 (1966) to support a rejection under § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. In the present case, the scope and content of the prior art, as evidenced by Miyasaka and Udayakumar, did not include the claimed subject matter, particularly the claimed memory cell comprising means for controlling means for storing data, the means for controlling comprising a silicon-rich insulator that injects current into a tunnel junction when the memory cell is selected. This subject matter is entirely outside the scope and content of the cited prior art. These differences between the cited prior art and the claimed subject matter are significant because, the claimed subject matter provides features and advantages not known or available in 16 and its dependent claims under 35 U.S.C. § 103 and *Graham*.

Claim 26:

Claim 26 recites:

> A memory cell made by a method comprising:
>
> a) providing a substrate,
>
> b) depositing and patterning a first conductive layer over the substrate,
>
> c) forming a storage layer over the patterned first conductive layer,
>
> d) forming a *layer of silicon-rich insulator* over the storage layer,
>
> e) forming a tunnel-junction layer over the layer of silicon-rich insulator, and

> f) forming and patterning a second conductive layer over the tunnel-junction layer, whereby a memory-cell stack is formed, the stack having a storage layer, *a silicon-rich insulator*, and a tunnel-junction layer in series relationship between the first and second conductive layers, whereby the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell, *wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected.*

(Emphasis added).

As demonstrated above in connection with claims 1 and 16, Miyasaka and Udayakumar utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected."

The final Office Action argues that this "'product by process'" claim does not yield a distinct structure from the prior art. (final Office Action, p. 5). This is clearly incorrect. As demonstrated above, the cited prior art does not teach or suggest a silicon-rich insulator that is disposed so as to be able to inject current into a tunnel-junction layer. This clearly demonstrates that the product produced by the process recited in claim 26 is physically and structurally different than the product taught by the cited prior art.

Under the analysis required by *Graham v. John Deere*, 383 U.S. 1 (1966) to support a rejection under § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. In the present case, the scope and content of the prior art, as evidenced by Miyasaka and Udayakumar, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator that injects current into a tunnel junction when the memory cell is selected. This subject matter is entirely outside the scope and content of the cited prior art. These differences between the cited prior art and the claimed subject matter are significant because, the claimed subject matter provides

features and advantages not known or available in 26 and its dependent claims under 35 U.S.C. § 103 and *Graham*.

Claim 38:

Claim 38 recites:

> A memory cell made by a method comprising:
>
> a) providing a substrate,
>
> b) depositing and patterning a first conductive layer over the substrate,
>
> c) forming a storage layer over the patterned first conductive layer,
>
> d) forming a layer of silicon-rich insulator over the storage layer,
>
> e) forming a tunnel-junction layer over the layer of silicon-rich insulator,
>
> f) forming and patterning a second conductive layer over the tunnel-junction layer,
>
> g) forming and patterning an interlayer dielectric over the storage layer,
>
> h) forming an opening through the interlayer dielectric and extending to the storage layer, and
>
> i) filling the opening through the interlayer dielectric with conductive material to form a middle electrode contiguous with the storage layer, wherein the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell, *and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected.*

(Emphasis added).

As demonstrated above in connection with claims 1 and 16, Miyasaka and Udayakumar utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected."

The final Office Action argues that this "'product by process'" claim does not yield a distinct structure from the prior art. (final Office Action, p. 6). This is clearly incorrect. As demonstrated above, the cited prior art does not teach or suggest a silicon-rich insulator that is

disposed so as to be able to inject current into a tunnel-junction layer. This clearly demonstrates that the product produced by the process recited in claim 38 is physically and structurally different than the product taught by the cited prior art.

Under the analysis required by *Graham v. John Deere*, 383 U.S. 1 (1966) to support a rejection under § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. In the present case, the scope and content of the prior art, as evidenced by Miyasaka and Udayakumar, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator that injects current into a tunnel junction when the memory cell is selected. This subject matter is entirely outside the scope and content of the cited prior art. These differences between the cited prior art and the claimed subject matter are significant because, the claimed subject matter provides features and advantages not known or available in 38 and its dependent claims under 35 U.S.C. § 103 and *Graham*.

Claim 47:

Claim 47 recites:

> A multilayer memory made by a method comprising:
>
> a) providing a substrate,
>
> b) depositing and patterning a first conductive layer over the substrate,
>
> c) forming a storage layer over the patterned first conductive layer,
>
> d) forming and patterning a first interlayer dielectric over the storage layer,
>
> e) forming an opening through the first interlayer dielectric and extending to the storage layer,
>
> f) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode,

g) forming a layer of silicon-rich insulator over at least the first interlayer dielectric, at least a portion of the silicon-rich insulator being disposed contiguous with the middle electrode,

h) forming a tunnel-junction layer over the layer of silicon-rich insulator,

i) forming and patterning a second conductive layer over the tunnel junction layer and disposed to overlay vertically at least a portion of the middle electrode, whereby a portion of the second conductive layer is aligned with some portion of the middle electrode, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell, and *wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected*,

j) forming and patterning a second interlayer dielectric over the patterned second conductive layer, whereby a substrate is formed for subsequent layers,

k) forming vias as required through the second interlayer dielectric, and

l) repeating steps b) through k) until a desired number of memory array layers have been formed.

(Emphasis added).

As demonstrated above in connection with claims 1 and 16, Miyasaka and Udayakumar utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected."

The final Office Action argues that this "'product by process'" claim does not yield a distinct structure from the prior art. (final Office Action, p. 7). This is clearly incorrect. As demonstrated above, the cited prior art does not teach or suggest a silicon-rich insulator that is disposed so as to be able to inject current into a tunnel-junction layer. This clearly demonstrates that the product produced by the process recited in claim 47 is physically and structurally different than the product taught by the cited prior art.

Under the analysis required by *Graham v. John Deere*, 383 U.S. 1 (1966) to support a rejection under § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in

view of the ordinary skill in the art. In the present case, the scope and content of the prior art, as evidenced by Miyasaka and Udayakumar, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator that injects current into a tunnel junction when the memory cell is selected. This subject matter is entirely outside the scope and content of the cited prior art. These differences between the cited prior art and the claimed subject matter are significant because, the claimed subject matter provides features and advantages not known or available in 47 and its dependent claims under 35 U.S.C. § 103 and *Graham*.

Claim 55:

Claim 55 recites:

> A multilayer memory made by a method comprising:
>
> a) providing a substrate,
>
> b) depositing and patterning a first conductive layer over the substrate,
>
> c) forming a tunnel-junction layer over the first conductive layer,
>
> d) forming a layer of silicon-rich insulator over the tunnel-junction layer,
>
> e) forming and patterning a first interlayer dielectric over the layer of silicon-rich insulator,
>
> f) forming an opening through the first interlayer dielectric and extending to the layer of silicon-rich insulator,
>
> g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode, at least a portion of the middle electrode being disposed contiguous with the silicon-rich insulator,
>
> h) forming a storage-element layer over the patterned first interlayer dielectric,
>
> i) forming and patterning a second conductive layer over the storage element layer, the patterned second conductive layer being disposed to overlay vertically at least a portion of the middle electrode, whereby a portion of the second conductive layer is aligned with some portion of the middle electrode, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell, and *wherein the silicon-*

rich insulator injects current into the tunnel-junction layer when the memory cell is selected,

j) forming and patterning a second interlayer dielectric over the patterned second conductive layer, whereby a substrate is formed for subsequent layers,

k) forming vias as required through the second interlayer dielectric, and

l) repeating steps b) through k) until a desired number of memory array layers have been formed.

(Emphasis added).

As demonstrated above in connection with claims 1 and 16, Miyasaka and Udayakumar utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected."

The final Office Action argues that this "'product by process'" claim does not yield a distinct structure from the prior art. (final Office Action, p. 7). This is clearly incorrect. As demonstrated above, the cited prior art does not teach or suggest a silicon-rich insulator that is disposed so as to be able to inject current into a tunnel-junction layer. This clearly demonstrates that the product produced by the process recited in claim 55 is physically and structurally different than the product taught by the cited prior art.

Under the analysis required by *Graham v. John Deere*, 383 U.S. 1 (1966) to support a rejection under § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. In the present case, the scope and content of the prior art, as evidenced by Miyasaka and Udayakumar, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator that injects current into a tunnel junction when the memory cell is selected. This subject matter is entirely outside the scope and content of the cited prior art. These differences between the cited prior

art and the claimed subject matter are significant because, the claimed subject matter provides features and advantages not known or available in 55 and its dependent claims under 35 U.S.C. § 103 and *Graham*.

In view of the foregoing, it is submitted that the final rejection of the pending claims is improper and should not be sustained. Therefore, a reversal of the Rejection of April 10, 2008 is respectfully requested.

Respectfully submitted,

DATE: July 30, 2008

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Rebecca R. Schow

VIII. CLAIMS APPENDIX

1. (Previously Presented) A memory array comprising:

a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and

b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals and having a storage element and a control element coupled in series between a row conductor and a column conductor, each control element including a tunnel junction and a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.

2. (Withdrawn) The memory array of claim 1, wherein the silicon-rich insulator of each memory cell is patterned.

3. (Original) The memory array of claim 1, wherein the silicon-rich insulator of each memory cell comprises silicon-rich oxide (SRO).

4. (Original) The memory array of claim 1, wherein the silicon-rich insulator of each memory cell is electrically isolated from the silicon-rich insulators of all other memory cells.

5. (Previously Presented) The memory array of claim 1, wherein the control element of each memory cell further comprises a tunnel junction layer thickness of about 3 – 5 nanometers.

6. (Original) The memory array of claim 1, wherein the storage element of each memory cell comprises an anti-fuse.

7. (Cancelled)

8. (Original) The memory array of claim 1, wherein the storage element of each memory cell comprises a tunnel junction.

9. (Original) The memory array of claim 1, wherein the storage element of each memory cell comprises a state-change layer.

10. (Original) The memory array of claim 9, wherein the state-change layer of the storage element comprises a chalcogenide.

11. (Original) The memory array of claim 1, wherein the row conductors are arranged in mutually orthogonal relationship with the column conductors.

12. (Withdrawn) A memory array comprising:

a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors arranged to cross at cross-points, and

b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals and having a storage element and a control element coupled in series between a row conductor and a column conductor,

each storage element comprising a tunnel-junction anti-fuse, and

each control element comprising a patterned silicon-rich insulator and a tunnel junction.

13. (Withdrawn) A memory cell comprising:

a storage element comprising a tunnel-junction anti-fuse, and

a control element coupled in series with the storage element, the control element comprising a patterned silicon-rich insulator and a tunnel junction.

14. (Withdrawn) The memory cell of claim 13. wherein the patterned silicon-rich insulator of the control element injects current into the tunnel junction of the control element when the memory cell is selected and isolates the storage element when the memory cell is unselected.

15. (Withdrawn) A memory array comprising:

a multiplicity of row conductors and a multiplicity of column conductors, the row conductors

and column conductors arranged to cross at cross-points, and

the memory cell of claim 13 disposed at each cross-point.

16. (Previously Presented) A memory array comprising:

a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and

b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals, each memory cell comprising means for storing data and means for controlling the means for storing data, the means for storing data and means for controlling being coupled in series between a row conductor and a column conductor, each means for controlling including a tunnel junction and a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.

17. (Withdrawn) A method for controlling a memory cell of the type having an anti-fuse storage element, the method comprising the steps of:

a) providing a patterned silicon-rich insulator combined with a tunnel junction to form a control element, whereby the memory cell is isolated when unselected,

b) coupling the control element in series with the anti-fuse storage element, and

c) providing conductive elements for supplying current to selectively inject current from the silicon-rich insulator into the tunnel junction of the control element when selecting the memory cell, wherein the memory cell has exactly two terminals.

18. (Withdrawn) A memory cell controlled in accordance with the method of claim 17.

19. (Withdrawn) A memory array comprising:

a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors arranged to cross at cross-points, and

the memory cell of claim 18 disposed at each cross-point.

20. (Withdrawn) A method for fabricating a memory cell, the method comprising the steps of:

a) providing a substrate,

b) depositing and patterning a first conductive layer over the substrate,

c) forming a storage layer,

d) forming a layer of silicon-rich insulator,

e) forming a tunnel-junction layer over the layer of silicon-rich insulator, and

f) forming and patterning a second conductive layer over the tunnel-junction layer, wherein the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell.

21. (Withdrawn) The method of claim 20, further comprising the step of patterning the layer of silicon-rich insulator.

22. (Withdrawn) The method of claim 20, further comprising the step of depositing an interlayer dielectric (ILD).

23. (Withdrawn) The method of claim 22, further comprising the step of planarizing the interlayer dielectric (ILD).

24. (Withdrawn) The method of claim 20, further comprising the step of forming a conductive electrode disposed contiguous with the layer of silicon-rich insulator.

25. (Withdrawn) The method of claim 24, further comprising the step of patterning the conductive electrode.

26. (Previously Presented) A memory cell made by a method comprising:

a) providing a substrate,

b) depositing and patterning a first conductive layer over the substrate,

c) forming a storage layer over the patterned first conductive layer,

d) forming a layer of silicon-rich insulator over the storage layer,

e) forming a tunnel-junction layer over the layer of silicon-rich insulator, and

f) forming and patterning a second conductive layer over the tunnel-junction layer, whereby a memory-cell stack is formed, the stack having a storage layer, a silicon-rich

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insulator, and a tunnel-junction layer in series relationship between the first and second conductive layers, whereby the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell, wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected.

27. (Original) A memory array comprising a multiplicity of the memory cells of claim 26.

28. (Original) A substrate carrying electronics comprising the memory array of claim 27.

29. (Original) An integrated circuit comprising the memory array of claim 27.

30. (Original) A multilayer memory comprising:

a) a multiplicity of the memory arrays of claim 27, arranged in memory layers,

b) a multiplicity of interlayer dielectrics disposed to separate adjacent memory layers, and

c) conductive vias selectively extending through the interlayer dielectrics to selectively interconnect memory cells of the memory arrays.

31. (Original) A substrate carrying electronics comprising the multilayer memory of claim 30.

32. (Original) An integrated circuit comprising the multilayer memory of claim 30.

33. (Previously Presented) The multilayer memory of claim 30, wherein the memory cells of the multilayer memory are organized in sets, the memory cells of each set being disposed to overlay vertically at least a portion of an adjacent set, whereby some portion of the memory cells of each set are aligned vertically with each other.

34-35. (Cancelled)

36. (Withdrawn) A method for fabricating a multilayer memory, the method comprising the steps of:

i) performing the steps of claim 20 to form a first memory layer,

ii) depositing an interlayer dielectric, whereby a substrate for a subsequent memory layer is formed,

iii) performing steps b) through f) of claim 20, and

iiv) repeating steps ii) and iii) until a desired number of memory layers is formed.

37. (Withdrawn) The method of claim 20, further comprising the steps of:

g) forming and patterning an interlayer dielectric over the storage layer,

h) forming an opening through the interlayer dielectric and extending to the storage

layer, and

i) filling the opening through the interlayer dielectric with conductive material to form a middle electrode contiguous with the storage layer.

38. (Previously Presented) A memory cell made by a method comprising:

a) providing a substrate,

b) depositing and patterning a first conductive layer over the substrate,

c) forming a storage layer over the patterned first conductive layer,

d) forming a layer of silicon-rich insulator over the storage layer,

e) forming a tunnel-junction layer over the layer of silicon-rich insulator,

f) forming and patterning a second conductive layer over the tunnel-junction layer,

g) forming and patterning an interlayer dielectric over the storage layer,

h) forming an opening through the interlayer dielectric and extending to the storage layer, and

i) filling the opening through the interlayer dielectric with conductive material to form a middle electrode contiguous with the storage layer, wherein the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell, and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected.

39. (Original) A memory array comprising a multiplicity of the memory cells of claim 38.

40. (Original) A substrate carrying electronics comprising the memory array of claim 39.

41. (Original) An integrated circuit comprising the memory array of claim 39.

42. (Withdrawn) A method for fabricating a multilayer memory, the method comprising the steps of:

a) providing a substrate,

b) depositing and patterning a first conductive layer over the substrate,

c) forming a storage layer,

d) forming and patterning a first interlayer dielectric over the storage layer,

e) forming an opening through the first interlayer dielectric and extending to the storage layer,

f) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode,

g) forming a layer of silicon-rich insulator, at least a portion of the silicon-rich insulator being disposed contiguous with the middle electrode,

h) forming a tunnel-junction layer over the layer of silicon-rich insulator,

i) forming and patterning a second conductive layer over the tunnel-junction layer and disposed to overlay vertically at least a portion of the middle electrode, whereby the second conductive layer is at least partially aligned with the middle electrode, and wherein the first

and second conductive layers are adapted to provide exactly two terminals for control of the memory cell,

j) forming and patterning a second interlayer dielectric, whereby a substrate is formed for subsequent layers,

k) forming vias as required through the second interlayer dielectric, and

l) repeating steps b) through k) until a desired number of memory array layers have been formed.

43. (Withdrawn) The method of claim 42, further comprising the step of patterning the layer of silicon-rich insulator.

44. (Withdrawn) The method of claim 42, further comprising the step of planarizing the first interlayer dielectric.

45. (Withdrawn) The method of claim 42, further comprising the step of planarizing the second interlayer dielectric.

46. (Withdrawn) The method of claim 42, wherein the steps are performed in the order recited.

47. (Previously Presented) A multilayer memory made by a method comprising:

a) providing a substrate,

b) depositing and patterning a first conductive layer over the substrate,

c) forming a storage layer over the patterned first conductive layer,

d) forming and patterning a first interlayer dielectric over the storage layer,

e) forming an opening through the first interlayer dielectric and extending to the storage layer,

f) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode,

g) forming a layer of silicon-rich insulator over at least the first interlayer dielectric, at least a portion of the silicon-rich insulator being disposed contiguous with the middle electrode,

h) forming a tunnel-junction layer over the layer of silicon-rich insulator,

i) forming and patterning a second conductive layer over the tunnel-junction layer and disposed to overlay vertically at least a portion of the middle electrode, whereby a portion of the second conductive layer is aligned with some portion of the middle electrode, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell, and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected,

j) forming and patterning a second interlayer dielectric over the patterned second conductive layer, whereby a substrate is formed for subsequent layers,

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k) forming vias as required through the second interlayer dielectric, and

l) repeating steps b) through k) until a desired number of memory array layers have been formed.

48. (Original) A substrate carrying electronics comprising the multilayer memory of claim 47.

49. (Original) An integrated circuit comprising the multilayer memory of claim 47.

50. (Withdrawn) A method for fabricating a multilayer memory, the method comprising the steps of:

a) providing a substrate.

b) depositing and patterning a first conductive layer over the substrate,

c) forming a tunnel-junction layer over the first conductive layer,

d) forming a layer of silicon-rich insulator,

e) forming and patterning a first interlayer dielectric over the layer of silicon-rich insulator,

f) forming an opening through the first interlayer dielectric and extending to the layer of silicon-rich insulator,

g) filling the opening through the first interlayer dielectric with conductive material to

form a middle electrode, at least a portion of the middle electrode being disposed contiguous with the silicon-rich insulator.

h) forming a storage-element layer,

i) forming and patterning a second conductive layer over the storage-element layer and disposed to overlay vertically at least a portion of the middle electrode, whereby the second conductive layer is at least partially aligned with the middle electrode, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell,

j) forming and patterning a second interlayer dielectric, whereby a substrate is formed for subsequent layers,

k) forming vias as required through the second interlayer dielectric, and

l) repeating steps b) through k) until a desired number of memory array layers have been formed.

51. (Withdrawn) The method of claim 50, further comprising the step of patterning the layer of silicon-rich insulator.

52. (Withdrawn) The method of claim 50, further comprising the step of planarizing the first interlayer dielectric.

53. (Withdrawn) The method of claim 50, further comprising the step of planarizing the second interlayer dielectric.

54. (Withdrawn) The method of claim 50, wherein the steps are performed in the order recited.

55. (Previously Presented) A multilayer memory made by a method comprising:

a) providing a substrate,

b) depositing and patterning a first conductive layer over the substrate,

c) forming a tunnel-junction layer over the first conductive layer,

d) forming a layer of silicon-rich insulator over the tunnel-junction layer,

e) forming and patterning a first interlayer dielectric over the layer of silicon-rich insulator,

f) forming an opening through the first interlayer dielectric and extending to the layer of silicon-rich insulator,

g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode, at least a portion of the middle electrode being disposed contiguous with the silicon-rich insulator,

h) forming a storage-element layer over the patterned first interlayer dielectric,

i) forming and patterning a second conductive layer over the storage-element layer, the patterned second conductive layer being disposed to overlay vertically at least a portion of

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the middle electrode, whereby a portion of the second conductive layer is aligned with some portion of the middle electrode, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell, and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected,

j) forming and patterning a second interlayer dielectric over the patterned second conductive layer, whereby a substrate is formed for subsequent layers,

k) forming vias as required through the second interlayer dielectric, and

l) repeating steps b) through k) until a desired number of memory array layers have been formed.

56. (Original) A substrate carrying electronics comprising the multilayer memory of claim 55.

57. (Original) An integrated circuit comprising the multilayer memory of claim 55.

58. (Previously Presented) The memory array of claim 1, wherein the two terminals of the two-terminal memory cell disposed at each cross-point comprise the row conductor and column conductor respectively.

59. (Previously Presented) The memory array of claim 16, wherein the two terminals of the two-terminal memory cell disposed at each cross-point comprise the row conductor and column conductor respectively.

IX. Evidence Appendix

None

X. Related Proceedings Appendix

None

XI. Certificate of Service

None